

Amendments In The Claims

Claim 1 (~~canceled~~, allowed in the parent case, and shown here as a convenience to the Examiner);

1. A method of measuring a data signal to create an eye diagram of that signal, the method
- 2 comprising the steps of:
 - (a) setting a hits count to zero;
 - 4 (b) comparing the instantaneous voltage of a clock signal associated with the data
signal to a clock threshold voltage to produce a logical clock signal;
 - 6 (c) delaying the logical clock signal by a selected first amount to produce a delayed
logical clock signal;
 - 8 (d) comparing the instantaneous voltage of the data signal to be measured to a data
threshold voltage to produce a logical data signal;
 - 10 (e) delaying the logical data signal by a selected second amount to produce a delayed
logical data signal;
 - 12 (f) delaying the delayed logical clock signal by a selected third amount to produce a
doubly delayed logical clock signal;
 - 14 (g) capturing the value of the delayed logical data signal in response to the delayed
logical clock signal;
 - 16 (h) capturing the value of the delayed logical data signal in response to the doubly
delayed logical clock signal;
 - 18 (i) incrementing the hits count each time a value captured in step (g) is different to that
captured in step (h);
 - 20 (j) repeating steps (b) through (i) until a selected condition is satisfied;
 - (k) subsequent to step (j), storing the count of step (i) in a data structure indexed by
 - 22 the difference between the first and second amounts and by the data threshold
voltage;
 - 24 (l) repeating steps (a) through (k) with different combinations of the data threshold
voltage and difference between the first and second amounts; and
 - 26 (m) generating an eye diagram from the hits counts stored in the data structure.

Claim 2 (amended);

2. An eye diagram analyzer comprising:

a ~~variable~~ clock signal waveform delay circuit having an input for receiving a clock signal and an output producing a delayed clock signal that is delayed by a selected first amount and whose transitions in a selected direction serve as a time reference;

a threshold detector having a variable threshold, an input for receiving a data signal to be measured as an eye diagram and having an output producing a logical data signal;

a variable data signal waveform delay circuit having an input coupled to receive the logical data signal and an output producing a delayed logical data signal whose amount of delay is a swept second amount that can range from less than to more than first amount of delay;

a transition detection circuit coupled to the delayed clock signal and to the delayed logical data signal, and having an output producing a transition signal indicative of a transition in the delayed logical data signal occurring during a selected length of time subsequent to a transition in the selected direction within the delayed clock signal;

a counter coupled to the transition signal and that counts occurrences thereof; and

a memory whose content is organized as ~~aan eye diagram~~ data structure indexed by the signed difference in the first and second amounts of delay ~~delays for the variable clock signal waveform delay circuit and the variable data signal waveform delay circuit,~~ by the variable threshold, and that stores in an indexed location the number of counted occurrences that the data signal occupied the indexed location with an eye diagram.

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